Please amend the claims as follows.

IN THE CLAIMS:

1. (Currently Amended) A decoder, having an input signal with a predetermined frequency and a first output signal, comprising:

filter means for low pass filtering the input signal to provide a first filter output;

a first decimator coupled to the filter means for decimating the first filter output to reduce a sampling frequency of the input signal, the first decimator providing an output signal that contains a sum of left channel information and right channel information;

a multiplier for multiplying a predetermined value by the input signal to generate an intermediate signal, wherein the input signal has a pilot signal component and wherein the pilot signal component in the intermediate signal is a lower frequency than the pilot signal component in the input signal;

the ~~a~~ filter means ~~for~~ receiving the intermediate signal and ~~for~~ providing the pilot signal component as an output;

a phase ~~lock-loop~~ angle estimation means for receiving the pilot signal component from the output of said filter, said phase ~~lock-loop~~ estimation means determining an approximate phase of the pilot signal component of the input signal and generating at least one trigonometric function using the approximate phase of the pilot signal component of the intermediate signal;

quadrature mixer means coupled to the input signal for shifting the input signal from the predetermined frequency to a lower frequency by forming a pair of quadrature signals;

the filter means low pass filtering each of the pair of quadrature signals;

a second decimator coupled to the filter means for decimating a first of the pair of quadrature signals to provide a first quadrature mixer output;

a third decimator coupled to the filter means for decimating a second of the pair of quadrature signals to provide a second quadrature mixer output;

means for using the at least one trigonometric function, the first quadrature mixer output and the second quadrature mixer output to ~~phase align a first data component of the input signal and a second data component of the input signal and provide a phase aligned first data component~~ generate a phase aligned output signal that contains a difference of the left channel information and the right channel information; and

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means for using the ~~phase aligned first data component to generate the first~~ output signal that contains a sum of left channel information and right channel information and using the output signal that contains a difference of left channel information and right channel information to generate a left channel signal and a right channel signal, the means comprising dynamically controlled filters to vary bandwidth of the output signal that contains a sum of left channel information and right channel information and the output signal that contains a difference of left channel information and right channel information depending upon received signal conditions.

2. (Original) A decoder as in claim 1, wherein the at least one trigonometric function includes a sine function and a cosine function.

3. (Original) A decoder as in claim 1, wherein the predetermined value is retrieved from a table.

4. (Original) A decoder as in claim 3, wherein the predetermined value is a cosine value.

5. (Currently Amended) A decoder as in claim 1, wherein said ~~decoder has a second output signal~~ first decimator, second decimator and third decimator each decimate by approximately a same decimation factor.

6. (Currently Amended) A decoder as in claim 5, ~~wherein the first output signal is a right stereo channel and the second output signal is a left stereo channel, wherein the first data component is a difference between a left channel and a right channel, and wherein the second data component is a summation of the left channel and the right channel~~ further comprising a fourth decimator coupled between the filter means and the phase angle estimation means, the fourth decimator decimating the pilot signal component.

Cancel claim 7.

8. (Currently Amended) A decoder as in claim ~~7~~1, wherein said ~~stereo blender~~ means for using the output signal that contains a sum of left channel information and right channel information and using the output signal that contains a difference of left channel information and right channel information further comprises:

a first filter for providing a first filter output;

a second filter for providing a second filter output; ~~and~~

combining circuitry, coupled to said first filter and said second filter, said combining circuitry combining the first filter output and the second filter output to produce the ~~first and second output signals~~ left channel signal and the right channel signal; and

control circuitry coupled to the first filter and the second filter for modifying bandwidth of the first filter and the second filter in response to presence of adjacent signal interference and distortion of the input signal.

9. (Currently Amended) A decoder as in claim 8, wherein the control circuitry modifies bandwidth by varying filter coefficients of said first filter ~~are selectable;~~ and ~~filter coefficients of~~ said second filter ~~are selectable~~.

10. (Original) A decoder as in claim 8, wherein said first filter and said second filter are FIR filters.

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11. (Original) A decoder as in claim 1, wherein the decoder is used in a radio receiver.

12. (Original) A decoder as in claim 1, wherein the predetermined value is approximate to, but not equal to, a frequency of the pilot signal component in the input signal.

13. (Original) A decoder as in claim 12, wherein the predetermined value is within 3 kilohertz of the frequency of the pilot signal component in the input signal.

14. (Currently Amended) A decoder as in claim 1~~, further comprising:~~

~~a decimator, coupled between said filter and said~~ wherein said phase angle estimation means further comprises a phase lock loop.

15. (Currently Amended) A decoder as in claim 14, wherein said first decimator reduces ~~a frequency of the intermediate signal~~ sampling rate of the first filter output by a factor of five.

16. (Currently Amended) A decoder as in claim ~~15~~ 6, wherein said fourth decimator reduces ~~the frequency~~ sampling rate of the intermediate signal by a factor of 20.

17. (Currently Amended) A decoder as in claim 1, wherein said phase ~~lock loop~~ angle estimation means operates at a frequency less than one tenth ~~a~~ the predetermined frequency of the input signal.

18. (Currently Amended) A method for decoding an input signal using only digital circuitry, comprising:

receiving the input signal;

low pass filtering the input signal to provide a first output that contains a sum of left channel and right channel information;

multiplying a predetermined value by the input signal to generate an intermediate signal, the input signal having a pilot signal component that is also in the intermediate signal but reduced in frequency;

~~using a phase lock loop having feedback to estimate~~ estimating phase information of at least one component of the input signal using only digital circuitry~~, the phase lock loop receiving an intermediate signal having a phase value; and~~

~~completing decoding of the input signal to generated an output signal~~ to provide first and second trigonometric functions using approximate phase of the pilot signal component in the intermediate signal;

multiplying the first and second trigonometric functions with respective first and second outputs of quadrature mixers to form a second output that contains a difference of left channel and right channel information; and

blending the first output and the second output to provide a left channel signal and a right channel signal by using dynamically controlled filters to vary bandwidth of the first output and the second output depending upon received signal conditions.

19. (Currently Amended) A method as in claim 18, wherein the step of ~~using the phase lock loop~~ estimating phase information further comprises:

adding a predetermined phase correction to ~~the~~ a phase value of the intermediate signal to produce a resultant phase value, wherein the predetermined phase correction is a function of a delay of a portion of the digital circuitry.

20. (Currently Amended) A method as in claim 18, wherein the step of ~~using the phase lock loop~~ estimating phase information further comprises:

multiplying ~~the~~ a resultant phase value by a predetermined positive integer to produce a multiplied resultant phase value; and

providing the first and second trigonometric functions by determining ~~at least one trigonometric function~~ first and second trigonometric values of the multiplied resultant phase value.

21. (Currently Amended) A method for decoding an input signal having a predetermined frequency and containing information on a left channel L and a right channel R, the method comprising:

~~filtering a L+R signal to produce a filtered L+R signal, where L is the left channel and R is the right channel;~~

~~filtering a L-R signal to produce a filtered L-R signal; and~~

~~after filtering the L+R signal and the L-R signal, combining the filtered L+R signal and the filtered L-R signal to produce a left channel output signal and a right channel output signal~~

low pass filtering the input signal to provide a first filter output;

decimating the first filter output to reduce a sampling frequency of the input signal;

providing an output signal that contains a sum of left channel information and right channel information;

multiplying a predetermined value by the input signal to generate an intermediate signal, wherein the input signal has a pilot signal component and wherein the pilot signal component in the intermediate signal is a lower frequency than the pilot signal component in the input signal;

low pass filtering the intermediate signal and providing the pilot signal component as an output;

determining an approximate phase of the pilot signal component of the input signal and generating at least one trigonometric function using the approximate phase of the pilot signal component of the intermediate signal;

shifting the input signal from the predetermined frequency to a lower frequency and forming a pair of quadrature signals;

low pass filtering each of the pair of quadrature signals;

decimating a first of the pair of quadrature signals to provide a first quadrature mixer output;

decimating a second of the pair of quadrature signals to provide a second quadrature mixer output;

generating a phase aligned output signal that contains a difference of the left channel information and the right channel information; and

generating a left channel signal and a right channel signal by dynamically controlling filters to vary bandwidth of the output signal that contains a sum of the left channel information and the right channel information and the output signal that contains a difference of the left channel information and the right channel information depending upon received signal conditions.

22. (Currently Amended) A method as in claim 21, wherein all of said ~~step of~~ low pass filtering ~~the L+R signal and said step of filtering the L-R signal are~~ is performed using at least one FIR filter.

23. (Currently Amended) A method as in claim 21, wherein at least a portion of said step ~~of filtering the L+R signal and said step of~~ low pass filtering ~~the L-R signal are~~ is performed in software.

24. (Original) A method as in claim 23, further comprising:

providing software modifiable filter coefficients.